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CONFIRMATION NO. 9733

SERIAL NUMBER 10/774,406	FILING DATE 02/10/2004 RULE	CLASS 438	GROUP ART UNIT 2813	ATTORNEY DOCKET NO. 501.37465CC8	
APPLICANTS Yoshikazu Tanabe, Iruma-shi, JAPAN; Satoshi Sakai, Tokyo, JAPAN; Nobuyoshi Natsuaki, Tokyo, JAPAN; ** CONTINUING DATA ***** <i>yes/TSP</i> This application is a CON of 10/424,105 04/28/2003 which is a CON of 09/939,600 08/28/2001 PAT 6,596,650 which is a CON of 09/494,036 01/31/2000 PAT 6,518,201 which is a CON of 09/380,646 09/07/1999 PAT 6,239,041 which is a 371 of PCT/JP98/00892 03/04/1998 ** FOREIGN APPLICATIONS ***** <i>yes/TSP</i> JAPAN 9-50781 03/05/1997 IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 05/06/2004					
Foreign Priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 (a-d) conditions <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after met Verified and <i>Allowance</i> Acknowledged <i>[Signature]</i> <i>TSP</i> Examiner's Signature Initials		STATE OR COUNTRY JAPAN	SHEETS DRAWING 21	TOTAL CLAIMS 6	INDEPENDENT CLAIMS 1
ADDRESS 020457 ANTONELLI, TERRY, STOUT & KRAUS, LLP 1300 NORTH SEVENTEENTH STREET SUITE 1800 ARLINGTON, VA 22209-9889					
TITLE Method for fabricating semiconductor intergrated circuit device					
			<input type="checkbox"/> All Fees		